SYSTEM AND METHOD FOR ON-BOARD TIMING MARGIN TESTING OF MEMORY MODULES

ABSTRACT OF THE DISCLOSURE

A memory module includes several memory devices coupled to a memory hub. The memory hub includes several link interfaces coupled to respective processors, several memory controller coupled to respective memory devices, a cross-bar switch coupling any of the link interfaces to any of the memory controllers, a write buffer and read cache for each memory device and a self-test module. The self-test module includes a pattern generator producing write data having a predetermined pattern, and a flip-flop having a data input receiving the write data. A clock input of the flip-flop receives an internal clock signal from a delay line that receives a variable frequency clock generator. Read data are coupled from the memory devices and their pattern compared to the write data pattern. The delay of the delay line and frequency of the clock signal can be varied to test the speed margins of the memory devices.